Remarks

This Amendment is being submitted in consideration of placing the above-identified application in condition for formal allowability. Acceptance and formal entry therefor of the same is respectfully requested. (An authorized Credit Card Payment Form, covering the fee amount for the extended period of time, is enclosed herewith.)

The title was amended to be more aptly descriptive of the claimed subject matter. Acceptance of the same is respectfully requested.

Concurrently filed herewith is a paper entitled, "*Proposal to Amend the Drawings.*" Namely, the accompanying paper includes a proposal to label Figs. 31 and 32 as "Prior Art" illustrations, in keeping with the Examiner's requirement in item 3, on page 2 of the Office Action. Moreover, Fig. 4 of the drawings as it relates to the "fourth step" thereof is being amended to correct an informality and, therefore, also to overcome the objection directed thereto in item 4 on page 2 of the Office Action. That is, the "power supply film for electroplating" 16 which relates to the formation of the bump pad 3 and redistribution wire 4 in the "fifth step" in Fig. 4 was inadvertently omitted from the "fourth step" in Fig. 4 of the drawings. The Examiner is correct to note that the reference character 16 in the "fourth step" of Fig. 4 improperly points to the electrically insulating layer 5 (or stress relaxation layer). To reiterate, the reference character 5 in the drawings relates to the "stress relaxation layer", which is an electrically insulating layer. The reference 16, as described on page 24, lines 20-22 thereof, is intended to represent an "electric power supply film" used for electroplating in connection with the formation, also, of the "redistributing wire" 4 and a "bump pad" 3, such as shown with regard to the fifth step in Fig. 4 and described on page 24, line 25,

to page 25, line 3, of the Specification. Accordingly, in connection with effecting correction of this discovered informality, as noted by the Examiner, acceptance and formal entry of the revision to Fig. 4, as noted in red in the attachments to the accompanying paper, is respectfully requested. Since the proposed revisions to the drawings are directed to minor and formal matters, acceptance therefor of the accompanying proposal is respectfully requested. Formal implementation of the proposed amendments to the drawings will be effected upon formal approval thereof and in accordance with USPTO policy subsequently to applicants receiving an official Notification of Allowability of the above-identified application.

By the amendments presented hereinabove, previously non-elected claims 1-18 are being canceled but, however, applicants reserve their right to subsequently file a divisional application directed thereto.

Claims 19-38 were also canceled in favor in newly presented substitute claims 39-67. Therefore, the previously standing art rejections directed thereto were rendered moot. Likewise, the previously standing objection to claim 23 as well as the rejection of claims 24, 33 and 34 under 35 USC §112, second paragraph, were rendered moot in view of the canceling of those claims.

The newly presented claims 39-67 similarly cover a method for producing a semiconductor device as that intended to be covered by the now-canceled claims 19-38. That is, the substitute claims were presented in consideration of more clearly presenting the subject matter intended to be covered as well as to further define the invention including over that taught by the art documents cited in the previously standing art rejections. Also, any and all previously standing concern in terms of objections to the claims and/or questions of definiteness

were considered with regard to the drafting of the newly-presented claims. It is submitted, the invention according to substitute claims 39-67 not only is defining over Shimoishizaka et al (US 6,313,532) and Shirasaki (JP 05-175260) but, moreover, could not have been rendered obvious even in view of their combined teachings. The discussion below, it is submitted, supports this.

The present invention calls for a manufacturing scheme for a semiconductor device including the step of forming a stress relaxation layer on a semiconductor wafer (or semiconductor chip) by printing through using a mask. The major featured aspect covered by the mask printing (screen printing) according to the present invention includes:

(a) forming a stress relaxation layer that is sufficiently thick

(b) forming a stress relaxation layer by controlling formation of the inclined portion; and

(c) forming a stress relaxation layer in one step which is less costly than that compared with photolithography.

In accordance with the present invention, also, because "particles" are included in the electrically insulating material in the printing step, the insulating layer that is formed can lead to a characteristically improved electrically insulating layer (or stress relaxation layer). Additionally, as shown by the discussion on page 26 and 27 of the Specification and by the sketch which follows, a squeegee is moved to an opposite vertex of an opening portion in the mask and the electrically insulating layer (or stress relaxation layer) is formed, thereby the insulating layer is formed in a manner which also prevents the formation of voids.

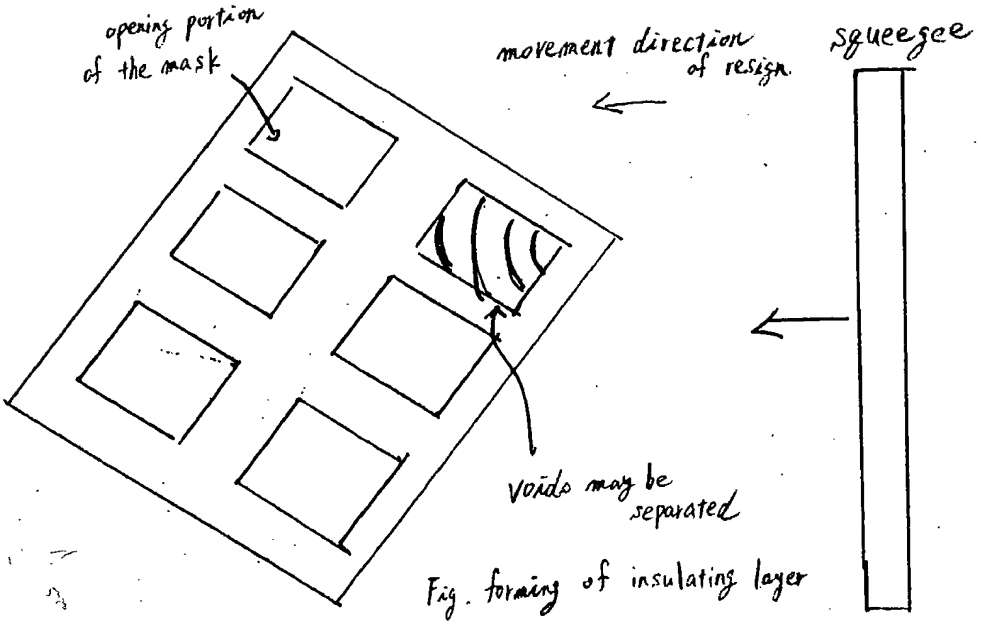


Fig. forming of insulating layer

Regarding the features discussed above, and insofar as relating to the present claimed subject matter, related discussion directed thereto is found in the following locations of the Specification: page 7, line 8, to page 8, line 6; page 26, line 1, to page 28, line 6; page 28, lines 12-26; page 30, line 27 to page 31, line 25; page 54, line 10, to page 55, line 4; page 79, line 28, to page 80, line 10, etc.

Shimoishizaka et al disclosed a manufacturing scheme for a semiconductor device having a stress relaxation layer. Figs. 3 - 4 of Shimoishizaka et al are directed to a method for forming a stress relaxation layer with an opening by plating a photosensitive insulating material and exposing/developing via scattered light, etc. Shimoishizaka et al, however, failed to disclose or suggest the forming of a stress relaxation layer by a mask printing process. The technique covered with regard to Figs. 3 - 4 in Shimoishizaka et al is described in column 7, line 19, to column 8, line 58, and, particularly, from line 31 to line 54 in column 7 thereof.

Shirasaki disclosed a scheme for improving production efficiency with regard to a method for sealing a semiconductor chip by a process including a sealing material consisting of liquid viscous resin by mask printing. However, Shirasaki failed to disclose a scheme calling for a mask printing process in the manufacture of a stress relaxation layer. It is noted, also, in Shirasaki, an incline portion is not formed at an edge of the sealing resin. This is because the insulating material in Shirasaki is used only for sealing the semiconductor device. Related discussion thereto is found in column 2, line 42 to column 3, line 14, of Shirasaki's Specification.

It is submitted, both Shimoishizaka et al and Shirasaki failed to disclose a method of manufacture for a semiconductor device having the main featured aspects as presently set forth in claims 39+, 53+, 65, 66 and 67. It is submitted, also, there is no teaching of why one of ordinary skill would have even attempted to combine the teachings of Shimoishizaka et al with that of Shirasaki. Nonetheless, even if one of ordinary skill would have attempted to combine the teachings of both disclosures, there still would not have been effected nor realizable therefrom a manufacturing scheme such as that called for according to claims 39+, 53+, 65, 66 and 67.

As noted above, insofar as the present invention is concerned, Shimoishizaka et al only disclosed the formation of a stress relaxation layer on a wafer by a process including plating the photosensitive insulating material followed by exposing/developing it. Shimoishizaka et al, it is submitted, neither disclosed nor suggested forming the stress relaxation layer by a mask printing process as that presently called for. Moreover, Shirasaki only disclosed using a mask printing process for sealing a resin in connection with improving production

efficiency. Shirasaki, it is submitted, neither disclosed nor suggested forming a stress relaxation layer on the wafer, as was earlier discussed.

Assuming, *arguendo,* that Shimoishizaka et al and Shirasaki are combinable, a semiconductor device having a relaxation layer and a wiring portion would be effected. However, once the semiconductor device is produced, the semiconductor device is then resin-sealed by mask printing. Clearly, therefore, such a method would not feature a stress relaxation layer that is formed by the process of mask printing. Moreover, there is no teaching or suggestion even in view of the combined teachings of Shimoishizaka et al and Shirasaki of forming such a stress relaxation layer with also an incline portion at the edge.

Turning to independent claims 39, 53 and 65, the invention therein calls for the formation of a stress relaxation layer formed by mask printing and, moreover, for the diffusing of particles therein. On the other hand, Shimoishizaka et al and Shirasaki, applied separately or even combinedly, failed to disclose or suggest forming the electrically insulating layer by mask printing an electrically insulating material with particles.

Shimoishizaka et al disclosed forming the stress relaxation layer by a process which includes exposing and developing after plating a photosensitive insulating film on a wafer. If an electrically insulating material with particles, as presently called for, is plated according to Shimoishizaka et al's scheme, the stress relaxation layer having a desired angle of inclination would <u>not</u> be formed because of the scattering of light resulting from the exposure process. That is, the present invention according to claims 39+, 53+ and 65 could not have been

achievable without prior knowledge of the type of material needed as that presently called for.

In accordance with a scheme as that presently called for, the following occur from forming an electrically insulating layer via mask printing process of an electrical insulating material including particles:
(a) the viscoelasticity of a material is adjustable so that it is available for using a paste, which leads to superior printing characteristics; (b) the thixotropy of the paste is controllable so that the printing characteristic is improved in conjunction with the viscosity; and (c) the inclination angle of a stress relaxation layer is adjustable. The formation of the stress relaxation layer, according to the present invention, does not require exposure so that light is not scattered in the stress relaxation layer. Such effects as that just described are discussed on page 30, lines 6-26, in the present specification.

Independent claims 66 and 67 call for a scheme in which, among other featured aspects thereof, the electrically insulating material is formed by moving a squeegee towards the direction of an opposite vertex in printing the electrically insulating material. In the printing process, a stress relaxation layer having high-reliability is formed. This is because voids are not formed when the paste is being filled in the opening portion of the mask. Such featured aspects, it is submitted, were not taught even in view of the combined teachings of Shimoishizaka et al and Shirasaki. Supportive discussion regarding this is found from page 26, line 1, to page 28, line 6, of the present Specification.

The invention according to claims 44 (dependent on claim 39) and 58 (dependent on claim 53) calls for the formation of a protrusive portion that is formed in the vicinity of a boundary of the flat portion and an incline portion in the

electrically insulating layer and that the protrusive portion is disposed over (*i.e.*, higher) a part of the flat portion. In accordance with the present invention, the protrusive portion is positively formed by such mask printing; therefore, the formation of wiring on the protrusive portion can be satisfactorily implemented without fear of breakage due to stress. Supportive discussion regarding this is found, for example, on page 31, line 26, to page 27, line 4, of the Specification.

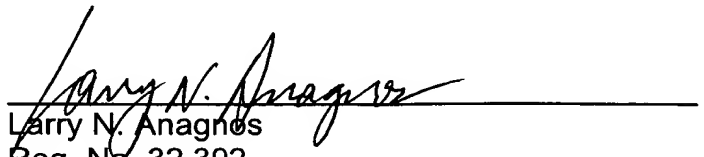
The invention according to claim 52 (dependent on claim 39) and claim 64 (dependent on claim 53) further calls for the electrically insulating material to be formed by a mask printing process which has smaller opening portions than that of the region covered by the electrically insulating layer. In accordance with such a scheme, the size of the mask openings must be smaller than the size of the actual electrically insulating layer in view of the spilling out of the electrically insulating material at the edge after removing the mask. As a result, therefor, the stress relaxation layer with the incline portion is able to be formed with high precision. Neither Shimoishizaka et al nor Shirasaki disclosed or suggested such featured aspects. Related discussion regarding this is found, for example, on page 26, lines 8-11, of the present Specification.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, favorable action therefor on the newly presented substitute claims 39-67 and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of

Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.39252X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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